RGPVNOTES.IN

Subject Name: **Basic Electrical and Electronics Engineering**

Subject Code: **BT-1004**

Semester: **1st / 2nd**

Department of Mechanical Engg.

Subject Name: Basic of Electrical and Electronics Engg. **Subject Code**: BT1004

Subject Notes

UNIT-5

Basic Electronics: Number systems and their conversion used in digital electronics, Demorgan's theorem,Logic Gates, half and full adder circuits, R-S flip flop, J-K flip flop. Introduction to Semiconductors, Diodes, V-I characteristics, Bipolar junction transistors (BJT) and their working, introduction to CC, CB and CE transistor configurations, different configurations and modes of operation of BJT.

NUMBER SYSTEMS:

BINARY NUMBER SYSTEM : - This number system has a base or radix of 2. The symbols or digits used in this system are 0 & 1.

OCTAL NUMBER SYSTEM : - This number system has a base or radix of 8. The symbols or digits used in this system are 0 through 7 i.e.(0, 1, 2, 3, 4, 5, 6, 7)

DECIMAL NUMBER SYSTEM :- This number system has a base or radix of 10. The symbols or digits used in this system are 0 through 9 i.e. (0, 1, 2, 3, 4, 5, 6, 7, 8, 9)

HEXADECIMAL NUMBER SYSTEM :- This number system has a base or radix of 16. The symbols or digits used in this system are 0 through F i.e. (0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F)

(1) BINARY TO DECIMAL CONVERSION:-

$(1111.11010)_2 = (?)_{10}$

Integeral part : $(1111)_2 = (1\times 2^3) + (1\times 2^2) + (1\times 2^1) + (1\times 2^0)$

$= 8 + 4 + 2 + 1$

$= 15$

ie. $(1111)_2 = (15)_{10}$

Fractional Part : $(0.11010)_2 = (1\times 1/2) + (1\times 1/4) + (0\times 1/8) + (1\times 1/16) + (0\times 1/32)$

$= 0.5 + 0.25 + 0 + 0.0625 + 0$

$= 0.8125$

ie. $(0.11010)_2 = (0.8125)_{10}$

Thus $(1111.11010)_2 = (15.8125)_{10}$

2) DECIMAL TO BINARY CONVERSION :-

$(15.812)_{10} = (?)_2$

Integeral part :

2	15	1
2	7	1
2	3	1
	1	

ie. $(15)_{10} = (1111)_2$

Fractional Part :

$(0.812\times 2) = 1.624 \rightarrow 1$

$(0.624\times 2) = 1.248 \rightarrow 1$

$(0.248\times 2) = 0.496 \rightarrow 0$

$(0.496\times 2) = 0.992 \rightarrow 0$

$(0.992\times 2) = 1.984 \rightarrow 1$

ie. $(0.812)_{10} = (0.11001)_2$

Thus (15 . 812)$_{10}$ = (1111 . 11001)$_2$

3) OCTAL TO DECIMAL CONVERSION:-

(57 . 245)$_8$ = (?)$_{10}$

Integeral part :

(57)$_8$ = (5 × 8^1) + (7 × 8^0)

= 40 + 7

= 47

ie. (57)$_8$ = (47)$_{10}$

Fractional Part :

(0.245)$_8$= (2× 1/8) + (4× 1/64) + (5× 1/512)

= 0.25 + 0.0625 + 0.0097

= 0. 3222

ie. (0.245)$_8$ = (0. 3222)$_{10}$

Thus (57.245)$_8$ = (47 . 3222)$_{10}$

4) DECIMAL TO OCTAL CONVERSION :-

(303 . 322)$_{10}$ = (?)$_8$

Integeral part :

8	303	7
8	37	5
	4	

ie. (303)$_{10}$ = (457)$_8$

Fractional Part :

(0.322 × 8)= 2.576 → 2

(0.576 × 8)= 4.608 → 4

(0.608 × 8)= 4.864 → 4

(0.864 × 8) = 6.912 → 6

(0.912 × 8)= 7.296 → 7

ie. (0 . 322)$_{10}$ = (0 . 24467)$_8$

Thus (303 . 322)$_{10}$ = (457 . 24467)$_8$

5) HEXADECIMAL TO DECIMAL CONVERSION :-

(EA6 . 2FA)$_{16}$ = (?)$_{10}$

Integeral part : (EA6)$_{16}$ = (E × 16^2) + (A × 16^1) + (6× 16^0)

= (14× 16^2) + (10 × 16^1) + (6× 1)

= 3584 + 160 + 6

= 3750

ie. (EA6)$_{16}$ = (3750)$_{10}$

Fractional Part : (0.2FA)$_{16}$ = (2× 1/16) + (F× 1/16^2) + (A× 1/16^3)

= (2× 1/16) + (15× 1/256) + (10× 1/4096)

= 0.125 + 0.0586 + 0.00244

= 0. 18604

ie. (0.2FA)$_{16}$ = (0. 18604)$_{10}$

Thus (EA6 . 2FA)$_8$ = (3750 . 18604)$_{10}$

6) DECIMAL TO HEXADECIMAL CONVERSION:

$(3750.365)_{10} = (?)_{16}$

Integeral part :

16	3750	6	→ 6
16	234	10	→ A
	14		→ E

ie. $(3750)_{10} = (EA6)_{16}$

Fractional Part :

$(0.365 \times 16) = 5.84 \rightarrow 5 \rightarrow 5$

$(0.84 \times 16) = 13.44 \rightarrow 13 \rightarrow D$

$(0.44 \times 16) = 7.04 \rightarrow 7 \rightarrow 7$

$(0.04 \times 16) = 0.64 \rightarrow 0 \rightarrow 0$

$(0.64 \times 16) = 10.24 \rightarrow 10 \rightarrow A$

ie. $(0.365)_{10} = (0.5D70A)_{16}$

Thus $(3750.365)_{10} = (EA6.5D70A)_{16}$

7) BINARY TO HEXADECIMAL CONVERSION:

$(1001111010100110.001011111010)_2 = (?)_{16}$

Integeral part :

$(1001111010100110)_2 = \{1001, 1110, 1010, 0110\}$

$= (\underbrace{1001}_{9}, \underbrace{1110}_{E}, \underbrace{1010}_{A}, \underbrace{0110}_{6})_2$

ie. $(1001111010100110)_2 = (9EA6)_{16}$

Fractional Part :

$(0.001011111010)_2 = \{\underbrace{0010}_{2}, \underbrace{1111}_{F}, \underbrace{1010}_{A},\}$

ie. $(0.001011111010)_2 = (0.2FA)_{16}$

Thus $(1001111010100110.001011111010)_2 = (9EA6.2FA)_{16}$

8) HEXADECIMAL TO BINARY CONVERSION:

$(99E.2FA)_{16} = (?)_2$

Integeral part :

$(99E)_{16} = \{\underbrace{9}_{1001} \quad \underbrace{9}_{1001} \quad \underbrace{E}_{1110}\} = (100110011110)_2$

ie. $(99E)_{16} = (100110011110)_2$

Fractional Part :

$(0.2FA)_{16} = \underbrace{2}_{0010}\ \underbrace{F}_{1111}\ \underbrace{A}_{1010} = (0.001011111010)_2$

Thus $(99E.2FA)_{16}$ = $(1001111010100110.001011111010)_2$

9) OCTAL TO BINARY CONVERSION:

$(404.245)_8 = (?)_2$

Integeral part :

$(404)_8 = \underbrace{4}_{100}\ \underbrace{0}_{000}\ \underbrace{4}_{100} = (100000100)_2$

ie. $(404)_8 = (100000100)_2$

Fractional Part :

$(0.245)_8 = \underbrace{2}_{010}\ \underbrace{4}_{100}\ \underbrace{5}_{101} = (0.010100101)_2$

Thus $(404.245)_8$ = $(100000100.010100101)_2$

10) BINARY TO OCTAL CONVERSION:

$(10011110.00101)_2$ = $(?)_8$

Integeral part :

$(10011110)_2 = \{010, 011, 110\} = (\underbrace{010}_{2}, \underbrace{011}_{3}, \underbrace{110}_{6})_2$

ie. $(10011110)_2 = (236)_8$

Fractional Part :

$(0.00101)_2 = \{\underbrace{001}_{1}, \underbrace{010}_{2}\}$

ie. $(0.00101)_2 = (0.12)_8$

Thus $(10011110.00101)_2$ = $(236.12)_8$

11) OCTAL TO HEXADECIMAL CONVERSION:

$(174654.273054)_8 = (?)_{16}$

Integeral part :

$(174654)_8 = \underbrace{1}_{001}\ \underbrace{7}_{111}\ \underbrace{4}_{100}\ \underbrace{6}_{110}\ \underbrace{5}_{101}\ \underbrace{4}_{100}$

$= (\underbrace{0000}_{0}, \underbrace{1111}_{F}, \underbrace{1001}_{9}, \underbrace{1010}_{A}, \underbrace{1100}_{C})_2$

ie. $(174654)_8 = (F9AC)_{16}$

Fractional Part : $(0.273054)_8 = \underbrace{010}_{2}\ \underbrace{111}_{7}\ \underbrace{011}_{3}\ \underbrace{000}_{0}\ \underbrace{101}_{5}\ \underbrace{100}_{4}$

$= (0.\underbrace{0101}_{5}, \underbrace{1101}_{D}, \underbrace{1000}_{8}, \underbrace{1011}_{B}, \underbrace{0000}_{0})$

ie. $(0.273054)_8 = (0.5D8B0)_{16}$

Thus $(174654.273054)_8 = (F9AC.5D8B)_{16}$

12) HEXADECIMAL TO OCTAL CONVERSION:

$(F9AC.5D8B)_{16} = (?)_8$

Integeral part :

$(F9AC)_{16} = \{1111\ 1001\ 1010\ 1100\} = (1111100110101100)_2$

ie. $(F9AC)_{16} = (1, 111, 100, 110, 101, 100)_2$

$= (001, 111, 100, 110, 101, 100)_2 = 174654$

ie. $(F9AC)_{16} = (174654)_8$

Fractional Part :

$(0.5D8B)_{16} = \{0101\ 1101\ 1000\ 1011\} = (0.010, 111, 011, 000, 101, 100)_2$

$= (\underbrace{010}_{2}, \underbrace{111}_{7}, \underbrace{011}_{3}, \underbrace{000}_{0}, \underbrace{101}_{5}, \underbrace{100}_{4})_2$

$= (0.273054)_8$

ie. $(0.5D8B) = (0.273054)_8$

Thus $(F9AC.5D8B)_{16} = (174654.273054)_8$

De Morgan's Theorem:

I Theorem : Complement of the sum is equal to the product of complements.

$(A+B)' = A'.B'$

II Theorem : Complement of the product is equal to the sum of complements.

$(A.B)' = A' + B'$

Note: Here the sum and product refer to the Boolean sum and Boolean product ie. AND and OR respectively.

Proof :

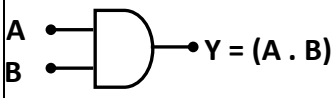
A	B	A'	B'	(A+B)	(A+B)'	(A'.B')	(A.B)	(A.B)'	A'+B'
0	0	1	1	0	1	1	0	1	1
0	1	1	0	1	0	0	0	1	1
1	0	0	1	1	0	0	0	1	1
1	1	0	0	1	0	0	1	0	0

Column for (A+B)' and A'.B' are same. Column for (A.B)' and A' + B' are same. **Hence proved.**

LOGIC GATES:

Logic Gates: Logic circuits that perform the logical operations are called gates. Gates are blocks of hardware that produce a logic-1 or logic-0 output signal if the input logic requirement are satisfied. Some of the logic gates are-

AND gate:
It is one of the basic logic gate whose output is high when all its input are high and output is low when any one of the input is low.



AND gate

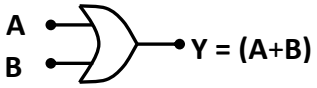
Inputs		Output
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Truth Table

Input A = Logic 0 or 1
Input B = Logic 0 or 1

Logic 0 = 0 Volt
Logic 1 = 5 Volt

OR gate:
It is one of the basic logic gate whose output is high when any one of its input is high and output is low when all inputs are low.



OR gate

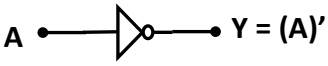
Inputs		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Truth Table

Input A = Logic 0 or 1
Input B = Logic 0 or 1

Logic 0 = 0 Volt
Logic 1 = 5 Volt

NOT gate: (Inverter)
It is one of the basic logic gate whose output is high when input is low and output is low when input is high.



NOT gate

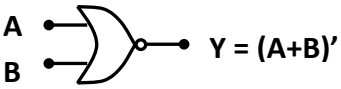
Input	Output
A	Y
0	1
1	0

Truth Table

Input A = Logic 0 or 1

Logic 0 = 0 Volt
Logic 1 = 5 Volt

NOR gate:
It is made up of two types of logic gates i.e. a combination of OR and NOT gate. Its output is high when all its input are low and output is low when any one of its inputs is high.



NOR gate

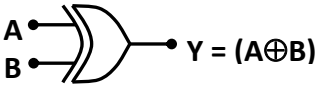
Inputs		Output
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Truth Table

Input A = Logic 0 or 1
Input B = Logic 0 or 1

Logic 0 = 0 Volt
Logic 1 = 5 Volt

EX-OR gate:
It has a graphical symbol similar to that of the OR gate, except for the additional curved line on the input side. Its output is low when all its input are high and for other input cases the outputs of EX-OR and OR gate are exactly same.



EX- OR gate

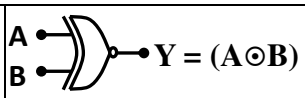
Inputs		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Truth Table

Input A = Logic 0 or 1
Input B = Logic 0 or 1

Logic 0 = 0 Volt
Logic 1 = 5 Volt

EX-NOR gate:
It is made up of two types of logic gates i.e. a combination of EX-OR and NOT gate. Its output is high when all its input are high and for other input cases the outputs of EX-NOR and NOR gate are exactly same.



EX- NOR gate

Inputs		Output
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Truth Table

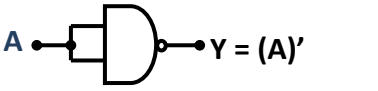
Input A = Logic 0 or 1
Input B = Logic 0 or 1

Logic 0 = 0 Volt
Logic 1 = 5 Volt

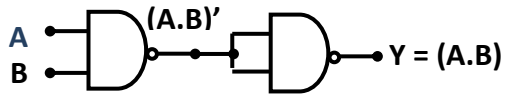
UNIVERSAL GATES:

NAND and NOR gates are called universal gates because it is possible to realize all basic (AND, OR and NOT) gates and derived gates using NAND and NOR gates.

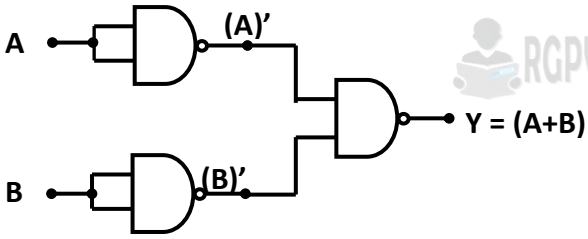
REALIZATION OF LOGIC GATES USING NAND GATES ONLY:



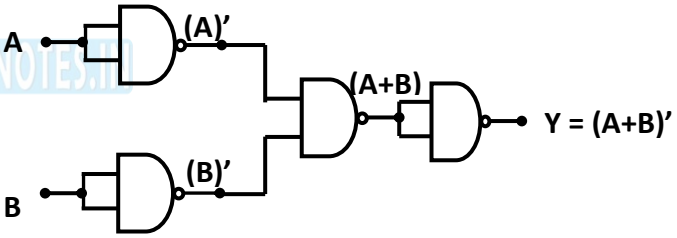
NAND gate as NOT gate



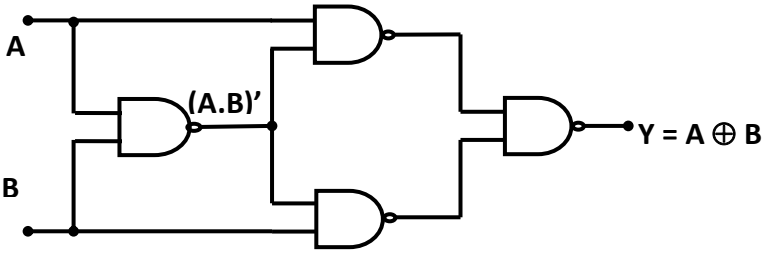
NAND gate as AND gate



NAND gate as OR gate

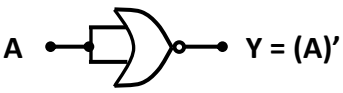


NAND gate as NOR gate

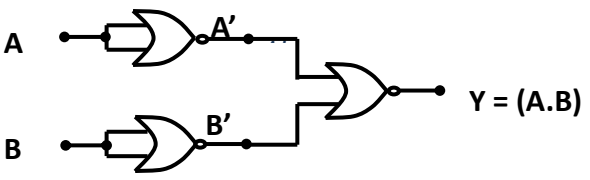


NAND gate as Ex-OR gate

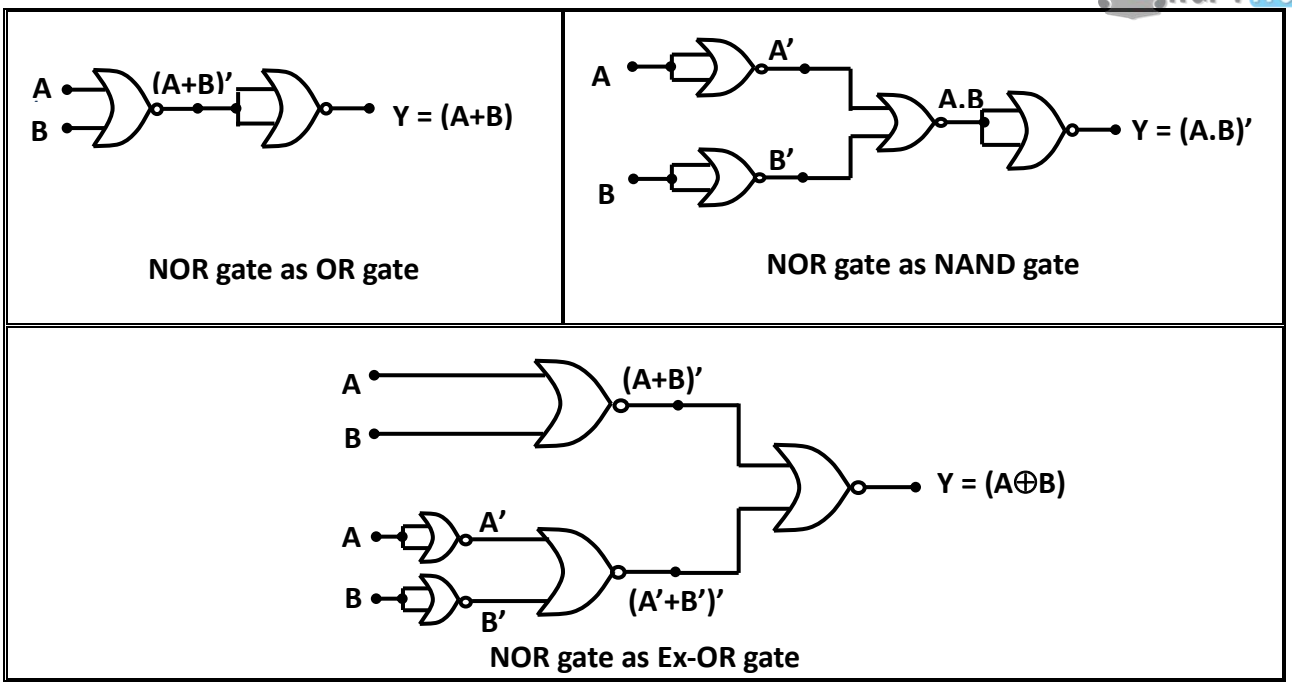
REALIZATION OF LOGIC GATES USING NAND GATES ONLY:



NOR gate as NOT gate



NOR gate as AND gate



BINARY ARITHMETIC:

BINARY ADDITION:-

1) 0 + 0 = Sum 0 with carry of 0.
2) 0 + 1 = Sum 1 with carry of 0.
3) 1 + 0 = Sum 1 with carry of 0.
4) 1 + 1 = Sum 0 with a carry of 1.
5) 1 + 1 + 1 = Sum 1 with carry of 1.

Example: Add $(111011.1101)_2$ with $(011111.0110)_2$

	1	1	1	1	1	1		1				**carry**
	1	1	1	0	1	1	.	1	1	0	1	**Augend**
+	0	1	1	1	1	1	.	0	1	1	0	**Addend**
1	0	1	1	0	1	1	.	0	0	1	1	**sum**

BINARY SUBTRACTION:

The basic principles of binary subtraction include the following:
A) 0 − 0 = 0. **B)** 1 − 0 = 1. **C)** 1 − 1 = 0. **D)** 10 − 1 = 1 with a borrow of 1 from the next more significant bit.

Example: Subtract $(11111.011)_2$ from $(111011.1101)_2$

	1	1	1	0	1	1	.	1	1	0	1	**Minuend**
–	0	1	1	1	1	1	.	0	1	1	0	**Subtraend**
	0	1	1	1	0	0	.	0	1	1	1	**Difference**

BINARY MULTIPLICATION:

The basic rules of multiplication are listed as follows:

1) 0 × 0 = 0.
2) 0 × 1 = 0.
3) 1 × 0 = 0.
4) 1 × 1 = 1.

Example: Multiply $(10.11)_2$ by $(11)_2$

		1	0	.	1	1	**Multiplicand**
			X		1	1	**Multiplier**
		1	0	.	1	1	
+	1	0	1	.	1	0	
1	0	0	0	.	0	1	**Product**

BINARY DIVISION:

Example: Divide $(110001)_2$ by $(111)_2$

Divisor 111	110001-**Divident** –0111	111 **Quotient**
	01010 – 111	
	0111 – 111	
	0000-**Remainder**	

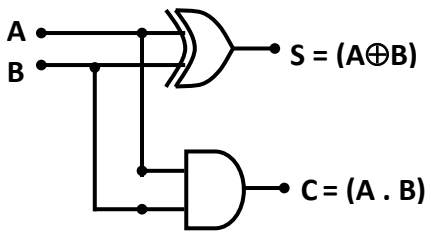
HALF ADDER: A combinational circuit that perform the addition of two bits is called half adder. This circuit needs two binary inputs and two binary outputs. The input variables, augend (X) and addend (Y) bits; the output variables SUM (S) and CARRY (C).

Truth Table:

INPUTS		**OUTPUTS**	
X	**Y**	**SUM (S)**	**CARRY(C)**
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

The simplified output Boolean function : **SUM (S) = X'.Y + X.Y' and CARRY (C) = X.Y**

The logic diagram of Half Adder :



FULL ADDER: When the augend and addend numbers contain more significant digits, the carry obtained from the addition of two bits is added to the next higher order pair of significant bits. The combinational circuit that performs the addition of three bits (two significant bits and a previous carry) is a full adder. It consists of three inputs (X and Y are actual 2-inputs and third input represents the $CARRY_{IN}$ (C_{IN}) generated from the previous lower significant bit position) and two outputs, SUM (S) and $CARRY_{OUT}$ (C_{OUT}).

Truth Table:

INPUTS			OUTPUTS	
X	Y	C_{IN}	SUM (S)	CARRY(C_{OUT})
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Boolean expression shown from the truth table which is shown:

SUM = $X'.Y'.C_{IN} + X'.Y.C_{IN}' + X.Y'.C_{IN}' + X.Y.C_{IN}$

SUM = $(X \oplus Y \oplus C_{IN})$

CARRY = $X'.Y.C_{IN} + X.Y.C_{IN}' + X.Y'.C_{IN} + X.Y.C_{IN}$

= $Y.C_{IN}(X + X') + X.Y.C_{IN}' + X.Y'.C_{IN}$ [Using Complement Law: X + X' = 1]

= $Y.C_{IN} + X.Y.C_{IN}' + X.Y'.C_{IN}$

= $Y(C_{IN} + C_{IN}'.X) + X.Y'.C_{IN}$ [Using Absorption Law: A+A'B = A+B]

= $Y(C_{IN} + X) + X.Y'.C_{IN}$

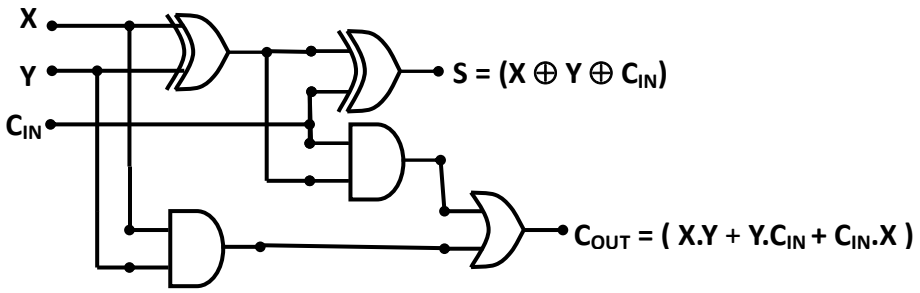
= $Y.C_{IN} + Y.X + X.Y'.C_{IN}$

= $C_{IN}(Y + X.Y') + Y.X$ [Using Absorption Law: A+A'B = A+B]

= $C_{IN}(Y + X) + Y.X$

CARRY = $C_{IN}.Y + C_{IN}.X + Y.X = X.Y + Y.C_{IN} + C_{IN}.X$

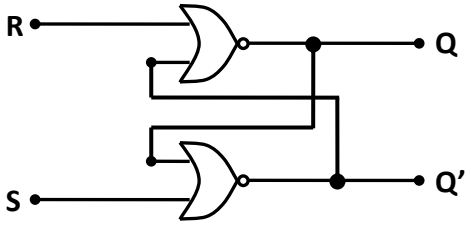
Logic Diagram of Full Adder using 2-half adder and OR gate:



FLIP- FLOPS:

A flip flop is a basic data storage element. A NAND or NOR gate individually act as a storage element when they are cross coupled with feedback. Such cross coupled NAND or NOR gates with feedback are known as flip flops. A flip flop is a bistable (output will remain permanently either 0 or 1 until it is forced to change the state by an external trigger) circuit. A flip flop have two outputs Q and Q', and are complement to each other.

R-S (RESET-SET)FLIP FLOP USING NOR GATES:

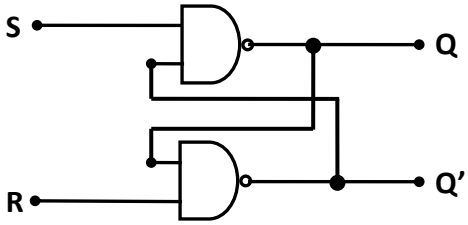


Truth Table:

S	R	Q (output)
0	0	No Change
1	0	1 (SET)
0	1	0 (RESET)
1	1	RACE

The truth table shown for NOR gate flip flop is similar to that of transistor flip flop.

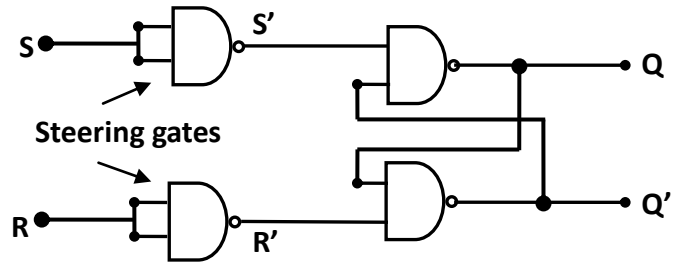
R-S (RESET-SET) FLIP FLOP USING NAND GATES:



Truth Table:

S	R	Q (output)
0	0	RACE
1	0	0 (RESET)
0	1	1 (SET)
1	1	No Change

The truth table shown for NAND gate flip flop is inverted to that of NOR gate flip flop, hence inverters gates are used to drive the inputs to the gates as shown:

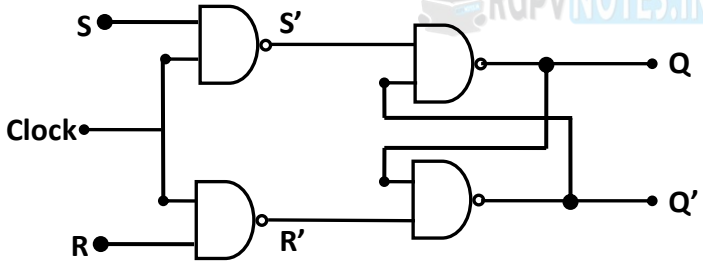


Truth Table:

S	R	Q (output)
0	0	No Change
1	0	1 (SET)
0	1	0 (RESET)
1	1	RACE

The truth table for NAND gate flip flop with inverters or steering gates or driving gates is similar to that of transistor flip flop, hence this flip flop is used to realize the desired practical flip flop.

CLOCKED R-S FLIP FLOP:



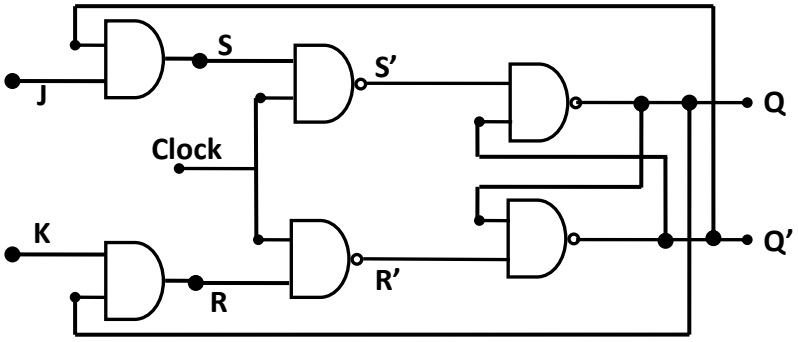
Truth Table:

Clock	S	R	Q (output)
0 or 1	0	0	No Change
1	1	0	1 (SET)
1	0	1	0 (RESET)
1	1	1	RACE

The clock signal or the enabling signal which makes the circuit to perform the required operation. If clock = 0, the circuit output will remain unchanged. If clock = 1, the flip flop is enabled and respond to the applied input signal.

J-K FLIP FLOP:

In order to overcome the invalid condition in R-S Flip Flop, the J-K Flip Flop is used.



Truth Table of J-K Flip Flop:

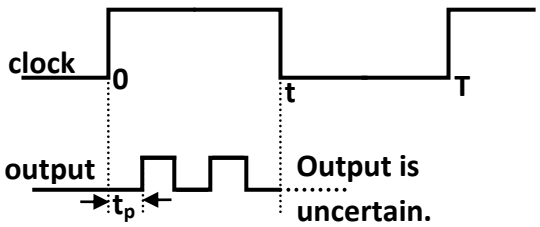
CLK	J	K	Qn	S	R	Q_{n+1} (output)	Remarks
1	0	0	0	0	0	0	Qn (No change)
1	0	0	1	0	0	1	
1	0	1	0	0	0	0	0 (RESET) (Make Q = 0)
1	0	1	1	0	1	0	
1	1	0	0	1	0	1	1 (SET) (Make Q = 1)
1	1	0	1	0	0	1	
1	1	1	0	1	0	1	Toggle or Complement
1	1	1	1	0	1	0	

Qn represent the past state; Q_{n+1} represent the present state i.e. the state of the output after the clock pulse is applied.

The J-input is analogous to the S input and K to the R input. So, when J=1 and K=0, the J-K flip flop is in SET state and when, J = 0 and K = 1, the flip flop is in RESET state. When J=K=1, the flip flop will complement its output condition, with high clock signal. This is the RACE around condition and it is a problem in JK flip flop. To overcome the problem of race around condition, Master-Slave JK flip flop is used.

RACE AROUND CONDITION:

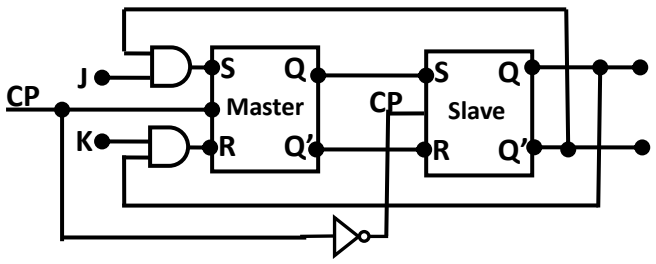
If J=K=1 and clock pulse =1, after a time interval t_p (propagation delay of NAND gates), output will change to Q=1. Now we have J=K=1 and Q=1. If the duration of clock pulse (T) is greater than t_p, then after another time interval t_p, the output will change back to Q=0, hence the output will oscillate between 0 and 1. This output is uncertain. This is race around condition.



Race around condition

MASTER-SLAVE FLIP FLOP:

The race around condition can be avoided, if the time duration of clock pulse (t) should be reduced than propagation delay of flip flop (t_p) ie. $t_p > t$, but practically it is not possible. A more practical method for this is the use of master-slave flip flop.



Master –Slave JK Flip Flop

The master is triggered when the clock (CP) is HIGH while the slave follows the master when the clock pulse is LOW.

INTRODUCTION TO SEMICONDUCTOR:

Insulators, Conductors and Semiconductors (with Energy Band Diagram)

Solid state materials can be classified into three groups: insulators, semiconductors and conductors. Insulators like diamond, have no free charge carriers available with them under normal conditions. Conducting materials like silver, have plenty of free electrons available for electric conduction. A semiconductor material like silicon, is one whose electrical properties lie in between those of insulators and good conductors. The electrical conduction properties of different elements can be explained in terms of the electrons having energies in the valence and conduction bands.

(i) Insulators

Insulators are those materials in which valence electrons are bound very tightly to their parents atoms, thus requiring very large electric field to remove them from the attraction of their nuclei. In other words, insulators have no free charge carriers available with them under normal conditions. In terms of energy bands, it means that insulators [Fig(a)] have a full valence band, have an empty conduction band, at room temperature . Have a large forbidden energy gap (of several Eg>6eV) between conduction and valence band, this means that a large amount of energy has to be supplied to the valence electron to push it into conduction band. But practically it is not possible, hence current is zero.

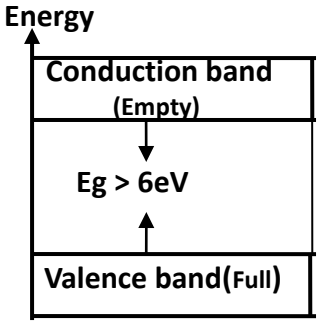


Figure: (a) Insulator

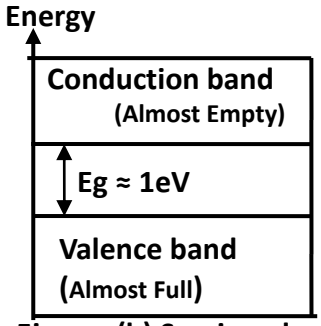


Figure: (b) Semiconductor

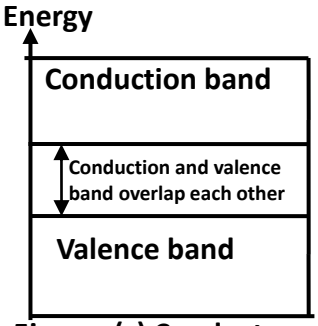


Figure: (c) Conductor

(ii) Conductors

Conducting materials has plenty of free electrons available for electric conduction. In terms of energy bands, it means that electrical conductors are those which have overlapping valence and conduction bands as shown in Fig (c). In fact, there is no forbidden energy gap between the two bands. Hence, at very low temperature there is the availability of large number of conduction electrons.

(iii) Semiconductors

A semiconductor material is one whose electrical properties lie in between those of insulators and good conductors. Examples are : germanium and silicon. In terms of energy bands, semiconductors can be defined as those materials which have almost an empty conduction band and almost filled valence band with a very narrow energy gap (of the order of 1 eV) . At 0°K, there are no electrons in the conduction band and the valence band is completely filled. However, with increase in temperature, width of the forbidden energy bands is decreased so that some of the electrons are liberated into the conduction band. In other words,

conductivity of semiconductors increases with temperature. Moreover, such departing electrons leave behind positive holes in the valence band. Hence, semiconductor current is the sum of electron and hole currents flowing in opposite directions.

PROPERTIES OF SEMICONDUCTOR MATERIAL :- A semiconductor is a material which exhibits the following properties :-

1) It has a resistivity lying between that of a conductor and an insulator.
2) It is tetravalent.
3) It exhibits negative temperature co-efficient of resistance .
4) It exhibits crystalline structure.
5) Its conductivity increases when doped with trivalent or penta valent atoms.

Silicon (atomic no. **14**) and Germanium (atomic no. **32**) are the two most important semiconductor materials.

EFFECT OF TEMPERATURE ON SEMICONDUCTORS:

(i) At absolute zero:

At absolute zero temperature, all the electrons are tightly held by the semiconductor atoms. The inner orbit electrons are bound whereas the valence electrons are engaged in co-valent bonding.At this temperature, the co-valent bonds are very strong and there are no free electrons. Therefore, the semiconductor behaves as a perfect insulator.

(ii) Above absolute zero:

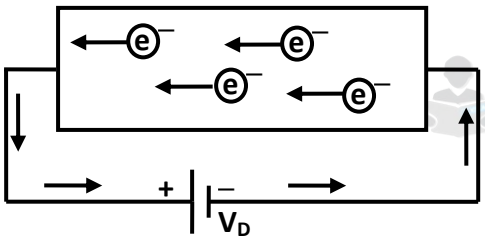


Figure: 01

When the temperature is raised, some of the co-valent bonds in the semiconductor break due to the thermal energy supplied.The breaking of bonds set those electrons, free, which are engaged in the formation of these bonds.These free electrons constitute an electric current if potential difference (V_D) is applied across the semiconductor. This is shown in figure 01. This shows that the resistance of a semiconductor decreases with the increase in temperature i.e. it has negative temperature co-efficient of resistance.

FLOW OF HOLE CURRENT IN A SEMICONDUCTOR:

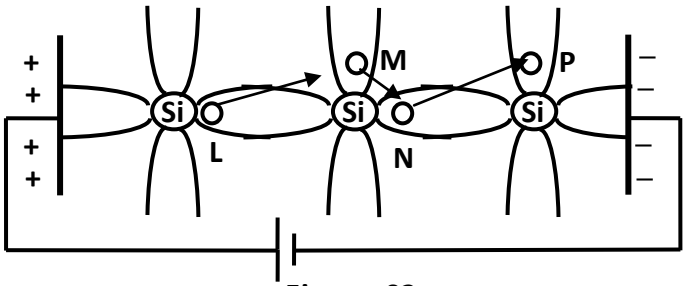


Figure: 02

At room temperature, some of the co-valent bonds in pure semiconductor break, setting up free electrons. Under the influence of electric field, these free electrons constitute electric current. At the same time, another current; hole current, also flows in the semiconductor.

When a covalent bond is broken due to thermal energy, the removal of one electron leaves a vacancy or hole (+charge) in the covalent bond. Therefore, thermal energy creates hole-electron pairs. That means number of free electrons is equal to number of holes. The current conduction by holes can be explained as follows: Suppose the valence electron at L ,in figure 02 has become free electron due to thermal energy. This creates a hole in the co-valent

bond a L. The hole is a strong centre of attraction for the electron. A valence electron at M from nearby co-valent bond comes to fill in the hole at L. This results in the creation of hole at M. Another valence electron at N in turn may leaves its bond to fill the hole at M, thus creating a hole at N.Thus the hole having a positive charge has moved from L to N i.e. towards the negative terminal of supply. This constitutes hole current.

INTRINSIC SEMICONDUCTOR:

A semiconductor in an extremely pure form is known as an intrinsic semiconductor. In an intrinsic semiconductor, even at room temperature, hole-electron pairs are created.

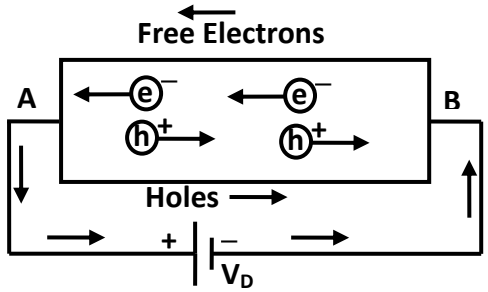


Figure: 03

When electric field is applied across an intrinsic semiconductor, the current conduction take place by free electrons and holes as shown in figure 03.The free electrons are produced due to the breaking up of some co-valent bonds by thermal energy. At the same time holes are created in the covalent-bonds. Under the influence of electric field, conduction takes place by both free electrons and holes.

Therefore,the total current inside the semiconductor is the sum of currents due to free electrons and holes. Referring to figure 03, holes being positively charged move towards the negative terminal of supply. As the holes reach the terminal B, electrons enter the semiconductor crystal near the terminal and combine with holes, thus cancelling them. At the same time, the loosely held electrons near the positive terminal A are attracted away from their atoms into the positive terminal.This creates new holes near the positive terminal which again drift towards the negative terminal. Since electron-hole pairs that are responsible for conduction of current in an intrinsic semiconductor are internal to the semiconductor crystal , the material is known as an intrinsic semiconductor.

EXTRINSIC SEMICONDUCTOR:

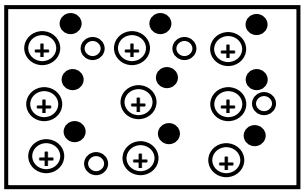
The conducting properties of an intrinsic semiconductor can be increased by adding small amount of suitable impurities to it (Doping Process). It is then called impurity or extrinsic semiconductor.Depending upon the type of impurity added, extrinsic semiconductor are classified into two types, such as: (i) n-type semiconductor (ii) p-type semiconductor

n-type Semiconductor:

When a small amount of pentavalent impurity (phosphorus, arsenic (As) or antimony(Sb)) is added to a pure semiconductor(1 part in 10 million), it is known as n-type semiconductor.The addition of pentavalent impurity provides a large number of free electrons in the semiconductor crystal.Such impurities which produce n-type semiconductor are known as donor impurities as they donate free electrons to the semiconductor crystal.

To explain the formation of n-type semiconductor, consider a pure germanium crystal. We know that germanium atom has four valence electrons. Arsenic is pentavalent i.e. its atom has five valence electrons. An arsenic atom fits in the germanium crystal in such a way that its four valence electrons form covalent bonds with four germanium atoms.The fifth valence electron of arsenic atom finds no place in co-valent bonds and thus remains free.

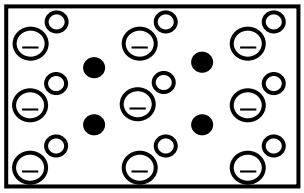
Therefore, for each arsenic atom added, one free electron will be available in the germanium crystal.The fifth left over valence electron of the pentavalent atom can not be accommodated in the valence band and travels to the conduction band.

 ⊕ Positive Immobile Ion O Hole (Minority Carrier) ● Free Electron(Majority Carriers) **Figure: 04**	The impurity atom loses one electrons and become a positive immobile ion. Thermal energy of room temperature still generated a few hole-electron pairs. However, the number of free electrons provided by the pentavalent impurity far exceeds the number of holes. Hence it is called n-type semiconductor (n stands for negative). So, n-type semiconductor has electrons as majority charge carriers and holes as minority charge carriers as shown in figure 04.

The current conduction in an n-type semiconductor is predominantly by free electrons i.e. negative charges and is called n-type or electron type conductivity.A n-type semiconductor is electrically neutral because the total number of positive charges is exactly equal to the total number of negative charges in the crystal.

P-type Semiconductor:

When a small amount of trivalent impurity (boron, indium or gallium) is added to a pure semiconductor, it is known as p-type semiconductor.The addition of trivalent impurity provides a large number of holes in the semiconductor crystal.Such impurities which produce p-type semiconductor are known as acceptor impurities as they accept electrons from the semiconductor crystal.To explain the formation of p-type semiconductor, consider a pure germanium crystal. We know that germanium atom has four valence electrons. Indium is tritavalent i.e. its atom has three valence electrons. An indium atom fits in the germanium crystal in such a way that its three valence electrons form covalent bonds with three germanium atoms.The absence of forth valence electron of indium atom creates a vacant site (hole) in one of the co-valent bonds. Therefore, for each indium atom added, one hole will be available in the germanium crystal.

 ⊖ Negative Immobile Ion O Hole (Majority Carrier) ● Free Electron(Minority Carriers) **Figure: 05**	The impurity atom accepts an electron and become a negative immobile ion. Thermal energy of room temperature still generated a few hole-electron pairs. However, the number of holes provided by the tritavalent impurity far exceeds the number of free electrons. Hence it is called p-type semiconductor (p stands for positive). So, p-type semiconductor has holes as majority charge carriers and electrons as minority charge carriers as shown in figure 05.

The current conduction in a p-type semiconductor is predominantly by holes i.e. positive charges and is called p-type or hole type conductivity. A p-type semiconductor is electrically neutral because the total number of positive charges is exactly equal to the total number of negative charges in the crystal.

FREE ELECTRONS OR CONDUCTION ELECTRONS :- When external energy is supplied to a semiconductor crystal in the form of light or heat (increase in temperature), some covalent bonds break and produce free electrons. Every free electron has an associated vacant site (hole) in the covalent bond. These free electrons are not under the control of any of the nuclei within the crystal. Since free electrons take part in the conduction of current , they are also known as conduction electrons. Conduction electrons or free electrons have energy levels much higher than valence electrons and take part in the conduction of current in a semiconductor.

VALENCE ELECTRONS OR BOUND ELECTRONS :- The outer most orbit electrons or valence electrons are shared by the neighboring semiconductor atoms to form covalent bonds in a

crystal. A valence electron is always associated with a particular nuclei and is under it's control, hence a valence electron is also known as a bound electron. A valence electron by itself cannot take part in the conduction of current. A valence electron will take part in the conduction of current only when there is hole movement, in other words hole movement is actually the movement of valence electrons in the valence band. At 0°K all the electrons in a silicon crystal exist as valence electrons (ie. there are no free electrons or holes) hence there is no current conduction and silicon behaves as an insulator.

DOPING :- The process of adding a calculated quantity ($1:10^8$) of trivalent or pentavalent atoms to an intrinsic semiconductor is known as doping. Doping helps in generating a single type of charge carrier (either free electrons or holes). Doping thus increases the conductivity of a semiconductor at room temperatures.

PN JUNCTION DIODE:

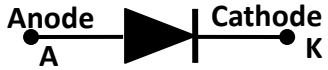


Figure: 06

A PN Junction Diode is basically a unidirectional device ie. passing current in only one direction only. However, unlike a resistor, a diode does not behave linearly with respect to the applied voltage, as the diode has an exponential current-voltage (I-V) relationship. The arrow head in the schematic symbol figure 06, of a p-n junction indicates the direction of conventional current flow when the diode is forward biased. P-N junction diode is fabricated using a single semiconductor crystal, in which one half is doped with p-type impurity and the other half with n-type impurity.

Operation of PN Junction Diode:

1.Unbiased Condition:

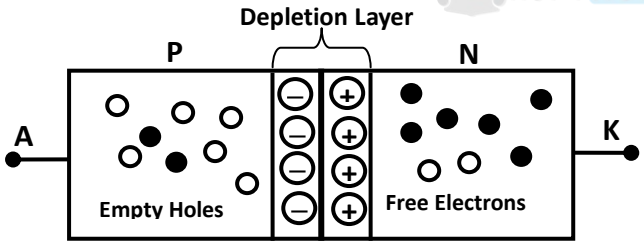


Figure: 07

Anode and cathode are at the same potential or at the zero potential. During formation of PN junction diode, electrons from n-type material diffuse into the p-type material and combine with holes. This process is called recombination.

This creates negative immobile ions near the junction in p-type material as shown in figure 07. Similarly, holes from p-type material diffuse into the n-type material and combine with electrons.This creates a positive immobile ions near the junction in n-type material.These two layers of positive and negative immobile ions form a depletion region near the junction. This term "depletion" means that the region is depleted of majority charge carriers.

2. Forward Biased Condition:

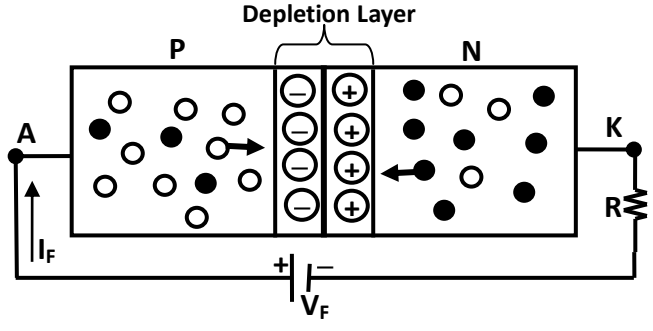


Figure: 08

Biasing, refers to the application of DC voltage across the terminals of device to establish certain operating condition for the device. When the positive terminal of the battery is connected to the p-type material and the negative terminal of the battery is connected to the n-type material, such a connection is called forward bias shown in figure 08.

Above figure shows the p-n junction diode in forward bias condition. The p region is connected to the positive terminal and n region is connected to the negative terminal of the DC voltage source (V_F). A resistor is also connected in series with the diode to make sure the current in the circuit does not rise above the maximum limit and damage the diode. When the diode is forward biased, the electric field in the depletion region and the external electric field due the DC voltage source are in opposite direction. This reduces the effective/net electric field in the depletion region.Since the net electric field is now reduced due to forward bias, electrons and holes now crosses the junction and constitutes a current. The direction of current is from p-region to n-region.Since the positive terminal of the battery is connected to the p-region, the electrons experiences an attractive force and moves to the positive terminal of the V_F whereas holes attracted towards the negative terminal of V_F. Thus we can conclude that current flow takes place when the diode is forward biased.

Effect on depletion region due to forward bias

In forward bias condition, the net electric field rduces in the junction and the electrons can pass from n-region to the p-region. As more electrons now flows into the depletion region, the number of positive ions is reduced. Simillarly, holes pass from p-region to n-region through the depletion region, the number of negative ions also decreases. Hence the width of depletion region decreases due to reduction in the number of positive and negative ions.

Effect of barrier potential during forward bias

During the formation of P-N Junction diode, the electrons from n-type material starts to move towards p-type material and forms negative ions. Similarly the holes from the p-type material starts to move towards n-type material and forms positive ions. This separation of positive and negative ions creates an electric field. When the electric field becomes sufficiently strong, it prevents further movement of electrons and holes. This electric field act as barrier for further movement of electrons and holes. This potential is called **barrier potential.** The physical distance from one side of barrier to the other side is known as barrier width. The difference in potential between the two sides is known as the height of potential barrier.The potential barrier is approximately 0.7V for silicon diode and 0.3V for a germanium diode.When the diode is forward biased, the majority charge carriers in p and n regions are pushed towards the junction. Since electrons and holes enter the depletion region, it causes a reduction in depletion width and hence the height of potential barrier. The reduced potential barrier allows a few high energy electrons on n-side to cross the junction on to the p-side and constitute the small forward current**.** When the diode is forward biased, the voltage drop across the diode is in between 0.65 Volt to 1Volt (for Si diode).

3. Reverse Bias Condition: When the positive terminal of the battery is connected to n-type material and the negative terminal of the battery is connected to p-type material, such a connection is called reverse bias.

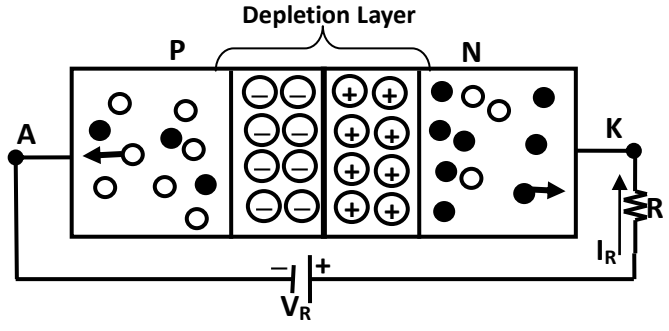


Figure: 09

In reverse bias condition, the negative terminal of the battery is connected to p-type material and the positive terminal of the battery is connected to n-type material.When the diode is reverse biased, the electric field due to the battery and the electric field of the depletion region are in the same direction which makes the net electric field more stronger.

So,the electrons from the n-type material (majority carriers) now faces a stronger electric field and it becomes even more difficult for them to move towards the p-type material. Simillarly, applicable for holes also. Hence conclude that there is no flow of current due to majority carriers when the diode is reverse biased.

Effect of reverse bias on the width of depletion region

When the positive terminal of the battery is connected to the n-type semiconductor, the electrons from the n-type semiconductor are quickly drawn towards the positive terminal. (Refer the above figure 09). This reduces the number of majority carriers in n-type semiconductor and additional positive ions are created. Similarly the holes from the p-type semiconductor are attracted towards the negative terminal of the battery. This reduces the number of holes in the p-type semiconductor and hence additional negative ions are created in the p-type material. Hence we conclude that as the number of positive and negative ions increases, the width of the depletion region increases. The diode offers very high resistance (1 to 2MΩ).

Reverse saturation current (I_R)

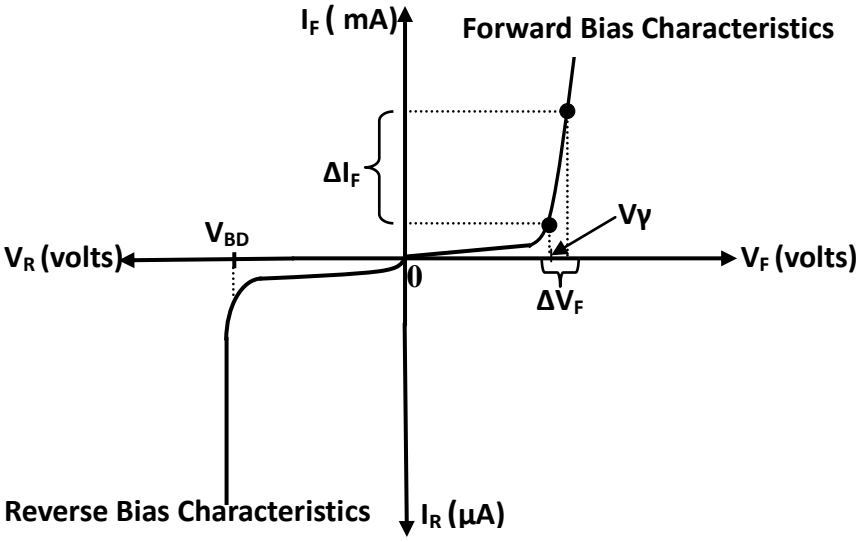
A very little current (in nano ampere range for silicon diode) flows due to minority carriers that are produced in the crystal due to thermal energy. When the diode is reverse biased, the electrons (minority carriers) from the p-type semiconductor are pushed towards the p-n junction by the negative terminal of the battery. Similarly the holes (minority carriers) from the n-type semiconductor are pushed towards the junction by the positive terminal of the battery. This movement of electrons and holes constitutes a current called reverse saturation current. The leakage current which has a very small value doubles itself for every 10°C rise in temperature. The term saturation is that, it reaches its maximum value very quickly and does not change significantly with increase in reverse bias potential.

Reverse breakdown voltage

When the reverse bias is increased beyond a certain limit, the reverse current increases drastically. The voltage beyond which the reverse current increases drastically is called reverse breakdown voltage. If left uncontrolled, this reverse current can cause physical breakdown of the junction. A p-n junction under reverse biased condition is therefore operated well within its breakdown voltage. Two mechanisms for diode breakdown are recognized- Avalanche breakdown and Zener breakdown.

V-I Characteristics of PN Junction Diode:

Forward Bias Condition: Initially when the forward bias voltage (V_F) is zero, the forward current (I_F) through the diode is also zero. When the forward bias voltage is gradually increased from zero to threshold voltage or cut-in voltage (V_γ) (0.3 V for germanium diode, 0.7 V for silicon diode)ie. $V_F = V_\gamma$, there is a gradual increase in the value of forward current.When the forward bias voltage is increased above threshold voltage, the current increases very rapidly with respect to voltage. The characteristics will be non-linear from the origin to Vγ because the total diode resistance $R_T = (R_J + R_B)$, where, R_J is the voltage dependent junction resistance and R_B is the voltage independent crystal bulk resistance. The characteristics is linear beyond Vγ because R_J becomes almost zero and only R_B remains. A small change in the value of forward bias voltage would result in large changes in the value of forward bias current. As it can be seen from the below graph, a small change in forward bias voltage ΔV_F results in drastic change in the value of forward current ΔI_F.



V-I Characteristics of PN diode

Reverse Bias Condition:

When the diode is reverse biased, leakage saturation current flows due to minority carriers. This current is of the order of nano-ampere to micro-ampere. This current does not change significantly with bias voltage. The current remains almost constant with the change in reverse bias voltage. When the reverse bias voltage is increased above reverse breakdown voltage, the current increases very rapidly. The graph above shows a plot of reverse bias voltage (V_R) vs current (I_R).

1.Graph from zero reverse bias voltage to breakdown voltage : Consider the graph shown above from zero reverse bias voltage to breakdown voltage. In this voltage range, the current remains almost constant. This current is called reverse saturation current (I_R).

2.Graph from breakdown voltage and above : If the reverse bias voltage is increased above the breakdown voltage, the diode is said to be in breakdown region and the current in the circuit increases drastically. It can be seen from the graph that even though the current increases drastically, the voltage remains almost constant.

DIFFUSION CURRENT: In the absence of an applied electric field, charges move from higher concentration region to a region of lower concentration, until equilibrium is established. This directional movement of charge carriers due to concentration gradient produces a component known as the diffusion current. Charge carriers can be electrons or holes.

Diffusion current density due to holes (J_P) = $-$ q.D_P.(dp/dx) A/m^2 where, q is the charge of an electron; D_P is diffusion constant of holes and (dp/dx) is the concentration gradient of holes.

Diffusion current density due to free electrons (J_n) = q.D_n.(dn/dx) A/m^2 where, q is the charge of an electron; D_n is diffusion constant of free electrons and (dn/dx) is the concentration gradient of free electrons.

DRIFT CURRENT: Drift current is defined as a flow of electric current caused by the movement of both electrons and holes when a semiconductor material is subjected to an electric field.

Drift current density due to holes (J_P) = q.P.μ_P.E A/m^2 where, q is the charge of an electron; P is numberof holes/cm^3 ; μ_P is the mobility of holes and E is the applied potential difference in V/cm.

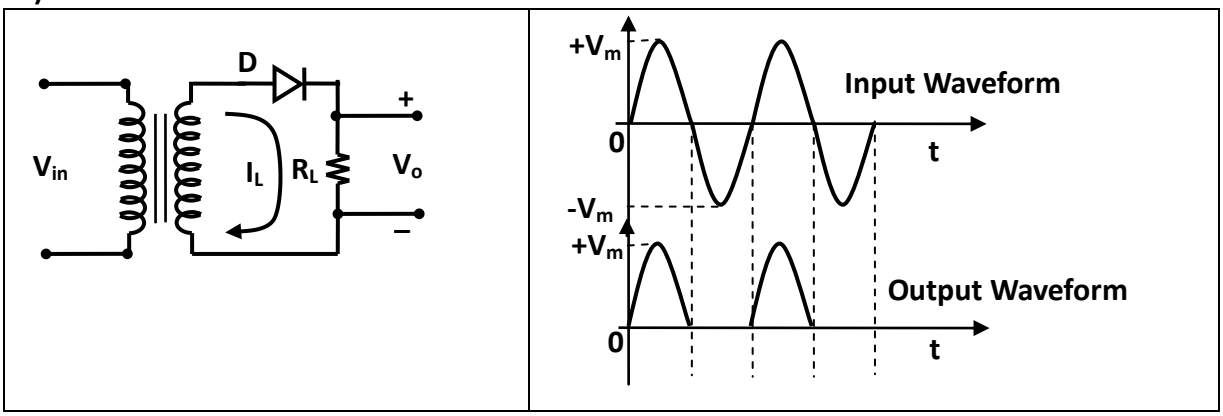
Drift current density due to electrons (J_n) = q.n.μ_n.E A/m^2 where, q is the charge of an electron; n is numberof electrons/cm^3 ; μ_n is the mobility of electrons and E is the applied potential difference in V/cm.

Total drift current density (J_{Drift}) = (J_P) + (J_n) = q.E.(n.μ_n + P.μ_P). From the expression of total

drift density it is seen that the magnitude of the drift current is directly proportional to the charge carrier concentration and magnitude of applied electric field.

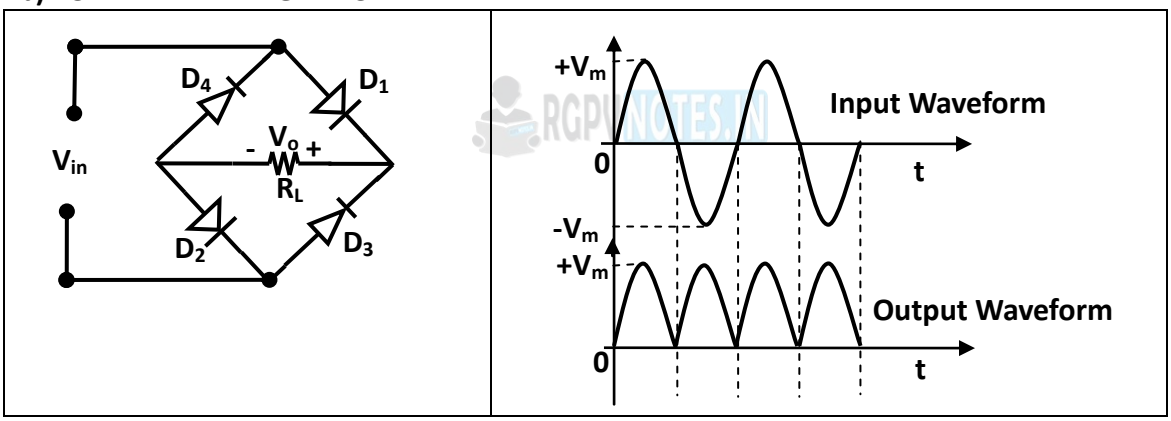
Applications of P-N Junction diode:

a)HALF WAVE RECTIFIER:



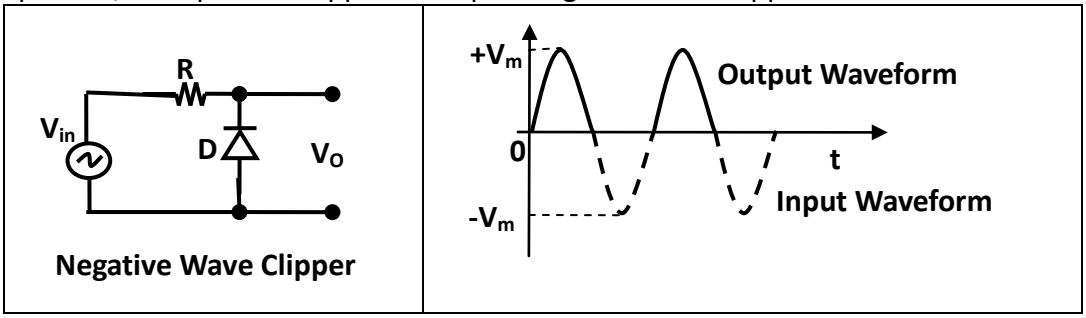
Rectifier is a circuit which converts AC signal into pulsating DC signal. Figure shows the circuit diagram of half wave rectifier. During positive half cycle, diode D is forward biased, so the output voltage(V_o) follows the input voltage (V_{in}). During negative half cycle, diode D is reverse biased, so the output voltage(V_o) is zero. The circuit produces an output only during one of the input cycle, hence known as half wave rectifier. For half wave rectifier we have following important expressions: **$I_{DC} = I_m/\pi$, $I_{RMS} = I_m/2$, %η =40.6, Ripple factor = 1.21**

b) FULL WAVE BRIDGE RECTIFIER:



The circuit produces an output during both the half cycles, it is known as full wave bridge rectifier. The output frequency is twice the input frequency. For full wave rectifier we have following important expressions: **$I_{DC} = 2I_m/\pi$, $I_{RMS} = I_m/\sqrt{2}$, %η =81.2, Ripple factor = 0.48**

c) CLIPPER: A clipper is a diode network which can clip off a portion of the input signal without distorting the remaining waveform. Depending on the diode connected in the circuit, negative or positive clipper is obtained. If DC voltage is connected in series with diode it is known as biased clipper. If the diode is in series with the output terminals it is known as series clipper, if parallel, then parallel clipper. Example: Negative wave clipper



Bipolar junction transistors (BJT) and their working:

Bipolar transistor owes its name to the fact that the current is due to both electrons and holes in the device. BJT is a three-layer, two-junction and three terminal device. For the three layers, either a n-type layer is sandwiched between two p-layers (p-n-p transistor) or a p-layer sandwiched between two n-type layers (n-p-n transistor). Out of the two outer layers, one is heavily doped (emitter) and the other one is moderately doped (collector); the middle layer is lightly doped (base) and also it is very thin as compared with outer layers. The two junctions are called as emitter-base junction (J1) and the collector-base junction (J2). The emitter-base junction is always forward biased and collector base junction is always reverse biased. Figure 10and11 shows npn and pnp transistor construction and symbol.E-Emitter;B-Base;C- Collector

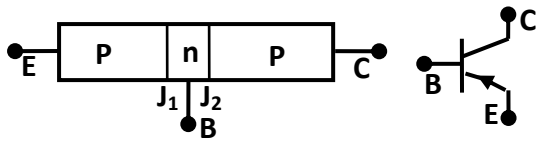


Figure 10: p-n-p transistor

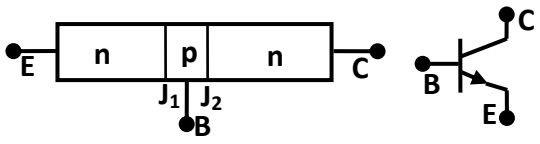


Figure 11: n-p-n transistor

Principle of operation of BJT:

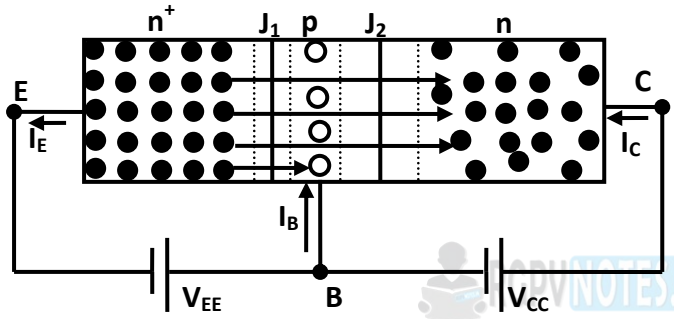


Figure shows the DC supply connection and current directions in a npn transistor. V_{EE} forward bias the emitter-base junction (J_1) and V_{CC} reverse bias the collector-base junction (J_2). I_C is the collector current, I_B is base current and I_E is emitter current.

n^+region is emitter (heavily doped), P-base region(thin region and lightly doped) and n-region is collector (large region and moderately doped). In a forward biased n^+- p junction (J_1) the current is primarily due to electrons injected from the n^+ to the p material. So, n^+p junction (J_1) may be regarded as a electron injecting device. Junction J_1 and J_2 share the same p- region. The injected electrons from the forward biased n^+p junction (J_1) will then participate in the reverse saturation current of the reverse biased p-n junction(J_2). The current from the emitter to collector is controlled by the base biasing and hence the base current. The requirement is that the electrons injected by the emitter should be available to constitute the collector current. So the sufficient care should be taken such that the electrons do not recombine with holes in the base region. Hence, the base region is made sufficiently narrow or thin. Also care should be taken to keep the electron life time large in the base region. The fundamental transistor equation is: $\mathbf{I_E = I_C + I_B}$. I_B is very small when compared to I_C (3 to 4% of I_C). Therefore $I_E \approx I_C$ ie. Input current = output current.

In a transistor, a large emitter current flowing through a low resistance input circuit is transferred into a high resistance collector circuit (output circuit), hence it is called a transfer-resistor or a transistor.

TRANSISTOR CONFIGURATIONS:

Transistor has only 3-leads hence depending on the lead that is common to both the input and output circuits there are three transistor configurations: 1) common base configuration 2) Common emitter configuration 3) Common collector configuration

COMMON BASE CONFIGURATION:

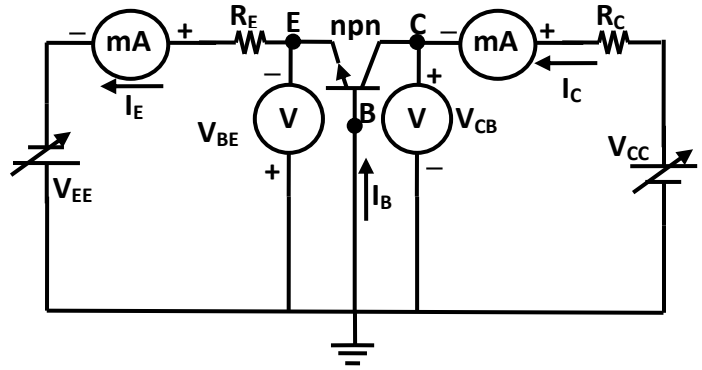
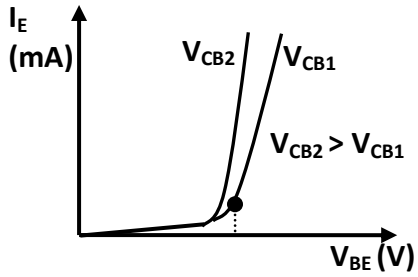
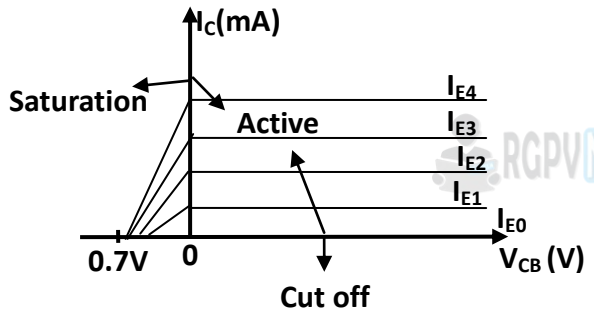


Figure shows the npn transistor connected in common base configuration. Here, input current is emitter current (I_E) and output current is collector current(I_C). Input voltage is V_{BE} and output voltage V_{CB}.



Input characteristics: Input characteristics is a plot of input voltage ,V_{BE} , v/s input current, I_E , keeping output voltage constant,V_{CB}. The dynamic input resistance r_i is obtained as:
$\mathbf{r_i = \Delta V_{BE} / \Delta I_E}$ keeping V_{CB} constant.



Output Characteristics: It is a plot of output voltage (V_{CB}) and output current (I_C) keeping input current (I_E) constant. From the family of curves we see that $I_C \approx I_E$ because I_B is very small. The slope of the output characteristics is almost zero, so the output resistance is very large. The dynamic output resistance $\mathbf{r_o}$ is obtained as:
$\mathbf{r_o = \Delta V_{CB} / \Delta I_C}$ keeping I_E constant.

Current gain of common base transistor is determined using relation: Alpha,$\boldsymbol{\alpha = \Delta I_C / \Delta I_E}$ keeping V_{CB} constant. The input resistance $\mathbf{r_i}$ has very low value (5 to 15Ω) while output resistance $\mathbf{r_o}$ has very high value (≈1MΩ). The current gain α has a value less than 1 (0.95 to 0.995). The voltage gain is high (150-200).

Applications: Transistor in C-B configuration is used as a wide band amplifier, a constant current source and a buffer amplifier (for impedance matching).

COMMON EMITTER CONFIGURATION:

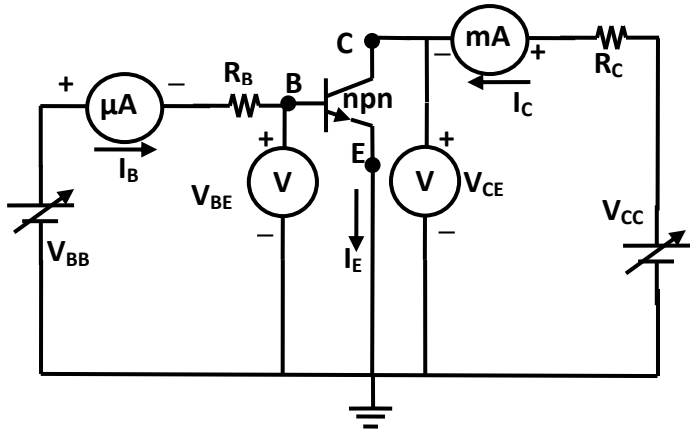
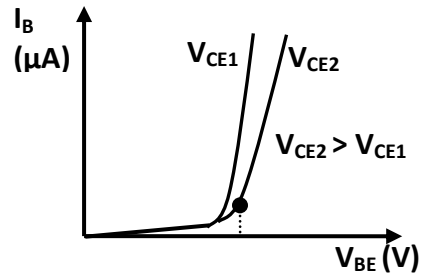
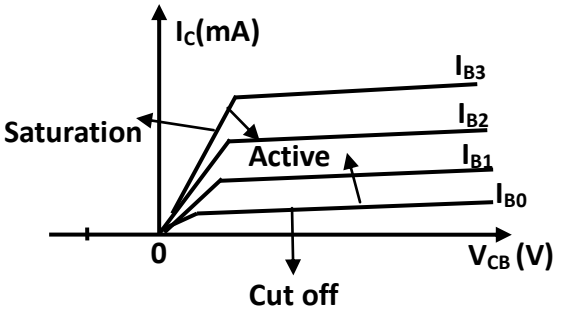


Figure shows the npn transistor connected in common emitter configuration. Here, input current is base current (I_B) and output current is collector current(I_C). Input voltage is V_{BE} and output voltage V_{CE}. V_{BB} is used to forward bias the B-E junction and V_{CC} is used to reverse bias the C-B junction (V_{CC}>V_{BB}).



Input characteristics: Input characteristics is a plot of input voltage ,V_{BE} , v/s input current, I_B , keeping output voltage constant,V_{CE}. The dynamic input resistance r_i is obtained as:
$\mathbf{r_i = \Delta V_{BE} / \Delta I_B}$ keeping V_{CE} constant.



Output Characteristics: It is a plot of output voltage (V_{CB}) and output current (I_C) keeping input current (I_B) constant. The slope of the output characteristics is appreciable, this means that output resistance is not as large as in case of C-B configuration. The dynamic output resistance $\mathbf{r_o}$ is obtained as:
$\mathbf{r_o = \Delta V_{CE} / \Delta I_C}$ keeping I_B constant.

Current gain of common emitter transistor is determined using relation: Beta, $\boldsymbol{\beta = \Delta I_C / \Delta I_B}$ keeping V_{CE} constant. The input resistance $\mathbf{r_i}$ is high (500Ω to 1.5kΩ) while output resistance $\mathbf{r_o}$ has a high value (15k to 50kΩ). The current gain β has a very large value (200 to 400). The voltage gain is high (250 to 500).

Applications: A transistor in C-E configuration is used as a voltage amplifier, power amplifier and multi-stage amplifier.

COMMON COLLECTOR CONFIGURATION:

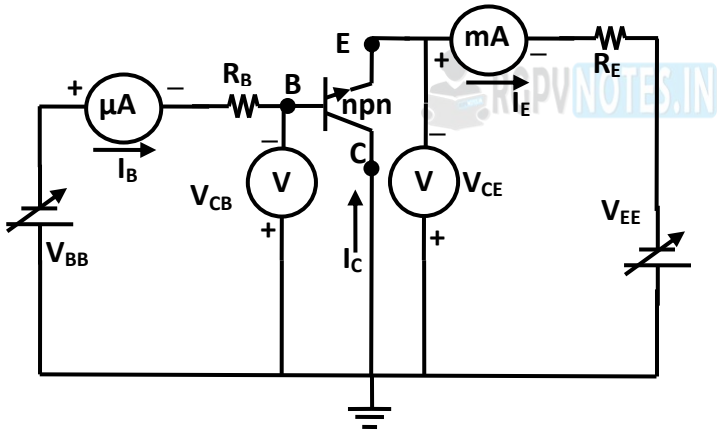
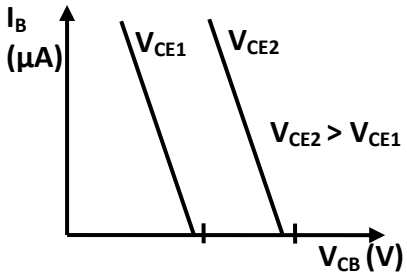
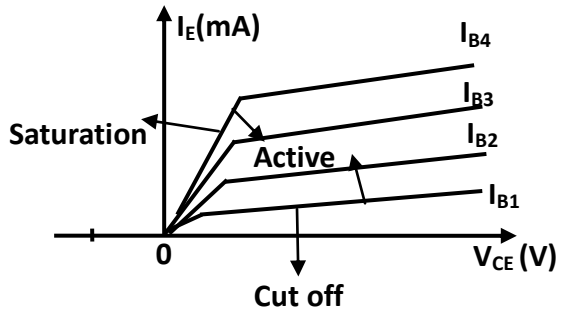


Figure shows the npn transistor connected in common collector configuration. Here, input current is base current (I_B) and output current is emitter current(I_E). Input voltage is V_{CB} and output voltage V_{CE}. Battery V_{EE} along with V_{BB} is used to forward bias the B-E junction ($V_{BB} > V_{EE}$).



Input characteristics: Input characteristics is a plot of input voltage ,V_{CB} , v/s input current, I_B , keeping output voltage constant,V_{CE}. The dynamic input resistance r_i is obtained as:
$\mathbf{r_i = \Delta V_{CB} / \Delta I_B}$ keeping V_{CE} constant.



Output Characteristics: It is a plot of output voltage (V_{CE}) and output current (I_E) keeping input current (I_B) constant. The slope of the output characteristics is appreciable, this means that output resistance is much smaller than that of the C-E configuration. The dynamic output resistance $\mathbf{r_o}$ is obtained as:

$\mathbf{r_o = \Delta V_{CE} / \Delta I_E}$ keeping I_B constant.

Current gain of common emitter transistor is determined using relation: Gamma, $\boldsymbol{\gamma = \Delta I_E / \Delta I_B}$ keeping V_{CE} constant. The input resistance $\mathbf{r_i}$ is high (≈ 1MΩ) while output resistance $\mathbf{r_o}$ has a very low value (less than 500Ω). The current gain (Gamma) **γ** has a very large value (β+1). The voltage gain is very low ($A_v \approx 1$).

Applications: A transistor in C-C configuration is used as a buffer amplifier to provide excellent impedance matching between two stages. The circuit is also known as an emitter follower.

Relationship between α and β:

1)α in terms of β: Since, Current gain of a transistor in C-B configuration, $\alpha = \Delta I_C / \Delta I_E$ and Current gain of a transistor in C-E configuration, $\beta = \Delta I_C / \Delta I_B$.

Basic transistor equation: $I_E = I_C + I_B$ ----------(1)

Considering the incremental values, we have, $\Delta I_E = \Delta I_C + \Delta I_B$----------(2)

Divide equation-2 by ΔI_C ie. $[\Delta I_E / \Delta I_C] = [\Delta I_C / \Delta I_C] + [\Delta I_B / \Delta I_C]$----------(3)

But, $[\Delta I_E / \Delta I_C] = 1 / \alpha$ and $[\Delta I_B / \Delta I_C] = 1 / \beta$

So, equation-3 becomes- $(1 / \alpha) = 1 + (1 / \beta)$.----------(4)

So, $\alpha = \beta / (\beta + 1)$.

2)β in terms of α: From equation -4, we have $(1 / \alpha) = 1 + (1 / \beta)$

So, $(1 / \beta) = (1 / \alpha) - 1$

Hence, $\beta = \alpha / (1 - \alpha)$

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